Abstract

A method of forming shallow trench isolation that reduces junction leakage at the boundary of shallow trench isolation and contact metallurgy of adjacent transistors and that avoids a reduction of carrier concentration in the source and drain region of transistors adjacent to the shallow trench isolation is described. The method to form a shallow trench isolation feature begins by providing a semiconductor substrate having a surface coated with at least one layer of an insulating material and a plurality of shallow trenches formed in the surface of the semiconductor substrate. A nitrogen doped insulating layer is then grown on the internal surfaces or sidewalls of the shallow trenches. A gap fill insulating layer is deposited upon the surface of the semiconductor substrate to fill the shallow trenches, and the gap fill insulating layer is planarized to remove excess material of the gap fill insulating layer from the surface of the semiconductor substrate while leaving the gap fill insulating layer within the shallow trenches.